WHAT IS CLAIMED IS:

1. A method comprising:

describing a representation of a first simulation model to a graphical user interface using hardware descriptions stored in a database;

receiving a response of the first simulation model to a first signal applied to the model; and

subsequently describing a second simulation model to the same graphical user interface.

2. The method of claim 1 further comprising receiving a response of the second simulation model to a second signal applied to the model.

3. The method of claim 2 wherein describing a second simulator model includes changing the hardware descriptions stored in the database.

4. The method of claim 1 wherein the simulation model represents a processor chip.

5. A method comprising:

causing functional processes to be associated with respective hardware descriptions stored in a database;

causing the functional processes to be implemented in a simulation model;

associating graphical user interface instructions with the hardware descriptions; and

causing the instructions to be used to simulate a chip design response on the graphical user interface.

6. The method of claim 5 including describing coupling of the functional processes in a first level of hierarchical relationships.

7. The method of claim 6 including causing the first level hierarchical relationships to be combined into a second level of hierarchical relationships.

8. The method of claim 7 further comprising repeatedly causing the combining of hierarchical relationships until the chip design is described.

9. The method of claim 5 wherein describing a second simulator model includes changing the hardware descriptions stored in the database.

10. The method of claim 5 wherein the chip design represents a processor chip.

11. An apparatus comprising:

a processor coupled to a memory storing instructions that cause the processor to:

associate functional processes with respective hardware descriptions stored in a database;

execute the functional processes in a simulation modeler;

associate graphical user interface instructions with the hardware descriptions; and

use the instructions to simulate a chip design response on a graphical user interface.

12. The apparatus of claim 11 wherein the hardware descriptions describe a coupling of the functional processes in a first level of hierarchical relationships.

13. The apparatus of claim 12 wherein the first level hierarchical relationships are combined into a second level of hierarchical relationships.

14. The apparatus of claim 13 wherein hierarchical relationships are repeatedly combined until the chip design is described.

15. The apparatus of claim 11 wherein the processor is configured to change the simulation model in response to a change in the hardware descriptions stored in the database.

16. The apparatus of claim 11 wherein the chip design represents a processor chip.

17. An article comprising a computer-readable medium storing computer-executable instructions for causing a computer system to:

associate functional processes with respective hardware descriptions stored in a database;

implement the functional processes in a simulation model;

associate graphical user interface instructions with the hardware descriptions; and

use the instructions to simulate a chip design response on the graphical user interface.

18. The article of claim 17 wherein the hardware descriptions describe a coupling of the functional processes in a first level of hierarchical relationships.

19. The article of claim 18 wherein the first level hierarchical relationships are combined into a second level of hierarchical relationships.

20. The article of claim 19 wherein hierarchical relationships are repeatedly combined until the chip design is described.

21. The article of claim 17 wherein the computer system is configured to change the simulation model in response to a change in the hardware descriptions stored in the database.

22. The article of claim 17 wherein the chip design represents a processor chip.